AMENDED CLAIMS SHOWING CHANGES

The amended claims are show below with bracketing and underlining.

38.   (Amended) A computer system for fetching, decoding and executing instructions comprising:

storage circuitry for holding a plurality of instructions at respective storage locations;

instruction fetch circuitry for fetching instructions from said storage circuitry, the instruction fetch circuitry including an indicator for providing an indication of a next address at which a next fetch operation is to be effected and a first and second instruction fetcher for fetching, respectively, a subsequent instruction and a new instruction; and

execution circuitry for executing fetched instructions comprising a branch instruction indicating a target location from which the subsequent instruction may be fetched, wherein said instruction fetch circuitry is operated responsive to execution of said branch instruction to fetch in parallel the subsequent instruction and the new instruction from said [target location] respective locations.

45.   (Amended) The computer system according to claim 38, wherein the branch instruction identifies a special register which holds an address from which [the] a first instruction of a string of new instructions is to be fetched.

49.   (Amended) The computer system according to claim 38, wherein the plurality of instructions are arranged in a plurality of instruction strings, each string comprising [the] a first instruction and [the] a plurality of subsequent instructions.